Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. (No amendments are made to the claims.)

Listing of Claims:

Claim 1 (Previously presented): A probe card assembly for electrically communicating test data between a semiconductor tester apparatus and a semiconductor device under test, said probe card assembly comprising:

a substrate configured to electrically contact said semiconductor tester apparatus,

a plurality of probes configured to electrically contact said semiconductor device under test, said plurality of probes located to a first side of said substrate,

a daughter card located to a second side of said substrate, and

an electric circuit at least a portion of which is disposed on said daughter card,

wherein said electric circuit receives as input test data received at said probe card assembly from one of said tester apparatus or said semiconductor device under test, enhances said test data, and outputs enhanced test data.

Claim 2 (Canceled)

Claim 3 (Previously presented): The probe card assembly of claim 1, wherein said electric circuit comprises at least one of a digital logic element, a microprocessor, an analog circuit element, a digital-to-analog converter, or an analog-to-digital converter.

Claim 4 (Canceled)

Claim 5 (Previously presented): The probe card assembly of claim 1, wherein said electric circuit enhances said test data by customizing at least a portion of said test data to test needs of said semiconductor device under test.

Claim 6 (Original): The probe card assembly of claim 5, wherein said test data comprises test signals generated by said semiconductor test apparatus and said electric circuit customizes at least a portion of said test signals.

Claim 7 (Original): The probe card assembly of claim 5, wherein said test data comprises response signals generated by said semiconductor device under test and said electric circuit customizes at least a portion of said response signals.

Claim 8 (Original): The probe card assembly of claim 1 further comprising a plurality of said daughter cards.

Claim 9 (Original): The probe card assembly of claim 8, wherein said plurality of daughter cards are disposed in stacked relationship to each other.

Claim 10 (Previously presented): The probe card assembly of claim 8, wherein at least a portion of said electric circuit is disposed on each of said plurality of daughter cards.

Claim 11 (Previously presented): The probe card assembly of claim 10, wherein said electric circuit comprises at least one of a digital logic element, a microprocessor, an analog circuit element, a digital-to-analog converter, or an analog-to-digital converter.

Claim 12 (Canceled)

Claim 13 (Previously presented): The probe card assembly of claim 10, wherein said electric circuit enhances said test data by customizing at least a portion of said test data to test needs of said semiconductor device under test.

Claim 14 (Original): The probe card assembly of claim 13, wherein said test data comprises test signals generated by said semiconductor test apparatus and said electric circuit customizes at least a portion of said test signals.

Claim 15 (Original): The probe card assembly of claim 13, wherein said test data comprises response signals generated by said semiconductor device under test and said electric circuit customizes at least a portion of said response signals.

Claim 16 (Original): The probe card assembly of claim 8, wherein said plurality of daughter cards includes at least three daughter cards.

Claim 17 (Previously presented): The probe card assembly of claim 16, wherein at least a portion of said electric circuit is disposed on each of said at least three daughter cards.

Claim 18 (Original): The probe card assembly of claim 16, wherein said at least three daughter cards are disposed in stacked relationship to each other.

Claim 19 (Previously presented): A method of making a probe card assembly, said method comprising:

providing a substrate including a plurality of tester contacts,

disposing a plurality of probes to a first side of said substrate, said probes configured to electrically contact a semiconductor device under test, and

disposing a daughter card to a second side of said substrate,

providing an electric circuit that receives as input test data received at said probe card assembly from one of said tester apparatus or said semiconductor device under test, enhances said test data, and outputs enhanced test data, and

disposing at least a portion of said electric circuit on said daughter card.

Claim 20 (Canceled)

Claim 21 (Previously presented): The method of claim 19, wherein said electric circuit comprises at least one of a digital logic element, a microprocessor, an analog circuit element, a digital-to-analog converter, or an analog-to-digital converter.

Claim 22 (Canceled)

Claim 23 (Previously presented): The method of claim 19, wherein said electric circuit enhances said test data by customizing at least a portion of said test data to test needs of said semiconductor device under test.

Claim 24 (Original): The method of claim 23, wherein said test data comprises test signals to be input into said semiconductor device under test and said electric circuit customizes at least a portion of said test signals.

Claim 25 (Original): The method of claim 23, wherein said test data comprises response signals generated by said semiconductor device under test and said electric circuit customizes at least a portion of said response signals.

Claim 26 (Original): The method of claim 19 further comprising securing a plurality of said daughter cards to said substrate.

Claim 27 (Original): The method of claim 26 further comprising securing said plurality of daughter cards to said substrate in stacked relationship to each other.

Claim 28 (Previously presented): The method of claim 26 further comprising disposing at least a portion of said electric circuit on each of said plurality of daughter cards.

Claim 29 (Previously presented): The method of claim 28, wherein said electric circuit comprises at least one of a digital logic element, a microprocessor, an analog circuit element, a digital-to-analog converter, or an analog-to-digital converter.

Claim 30 (Canceled)

Claim 31 (Previously presented): The method of claim 28, wherein said electric circuit enhances said test data by customizing at least a portion of said test data to test needs of said semiconductor device under test.

Claim 32 (Canceled)

Claim 33 (Original): The method of claim 31, wherein said test data comprises response signals generated by said semiconductor device under test and said electric circuit customizes at least a portion of said response signals.

Claim 34 (Original): The method of claim 26, wherein said plurality of daughter cards includes at least three daughter cards.

Claim 35 (Previously presented): The method of claim 34 further comprising disposing at least a portion of said electric circuit on each of said at least three daughter cards.

Claim 36 (Original): The method of claim 34 further comprising securing each of said at least three daughter cards to said substrate in stacked relationship to each other.

Claim 37 (Original): A probe card assembly made using the process of claim 19.

Claim 38 (Previously presented): A probe card assembly made using the process of claim 21.

Claim 39 (Previously presented): A probe card assembly made using the process of claim 23.

Claim 40 (Original): A probe card assembly made using the process of claim 26.

Claim 41 (Previously presented): A probe card assembly made using the process of claim 34.

Claim 42 (Previously presented): A probe card assembly comprising:

printed circuit means for electrically communicating with a semiconductor tester apparatus,

contact means for electrically communicating with a semiconductor device under test, said contact means being secured to a first surface of said printed circuit means,

electric circuit means for enhancing test data receive at said probe card assembly from one of said semiconductor tester apparatus or said semiconductor device under test, and

daughter card means for physically supporting at least a portion of said electric circuit means, said daughter card means secured to a second surface of said printed circuit means.

Claim 43 (Original): The probe card assembly of claim 42, wherein said daughter card means comprises a plurality of daughter cards in stacked relationship to each other, each of said plurality of daughter cards being substantially coplanar to said printed circuit means.

Claim 44 (Original): The probe card assembly of claim 43, wherein said plurality of daughter cards includes at least three daughter cards.

Claims 45 and 46 (Canceled)

Claim 47 (Previously presented): The probe card assembly of claim 42, wherein said electric circuit means enhances said test data by customizing said test data to meet test needs of said semiconductor device under test.

Claim 48 (Previously presented): The probe card assembly of claim 47, wherein said test data comprises test signals to be input into said semiconductor device under test and said electric circuit means customizes at least a portion of said test signals.

Claim 49 (Previously presented): The probe card assembly of claim 47, wherein said test data comprises response signals generated by said semiconductor device under test and said electric circuit means customizes at least a portion of said response signals.

Claim 50 (Previously presented): A probe card assembly for electrically communicating test data between a semiconductor test apparatus and a semiconductor device under test, said probe card assembly comprising:

a printed circuit board configured to electrically contact said semiconductor tester apparatus,

a plurality of probes configured to electrically contact said semiconductor device,

a daughter card secured to said printed circuit board, and

an electric circuit configured receive as input test data received at said probe card assembly from one of said tester apparatus or said semiconductor device under test, enhance said test data, and output enhanced test data, at least a portion of said electric circuit being disposed on said daughter card.

Claim 51 (Original): The probe card assembly of claim 50 further comprising a plurality of said daughter cards.

Claim 52 (Original): The probe card assembly of claim 51, wherein said daughter cards are disposed in stacked relationship to each other.

Claim 53 (Original): The probe card assembly of claim 51, wherein said plurality of daughter cards includes at least two daughter cards.

Claim 54 (Original): The probe card assembly of claim 51, wherein said plurality of daughter cards includes at least three daughter cards.

Claim 55 (Canceled)

Claim 56 (Previously presented): The probe card assembly of claim 50, wherein said test data comprises test signals generated by said semiconductor tester apparatus and said electric circuit processes at least a portion of said test signals.

Claim 57 (Previously presented): The probe card assembly of claim 50, wherein said test data comprises response signals generated by said semiconductor device and said electric circuit processes at least a portion of said response signals.

Claim 58 (Previously presented): The probe card assembly of claim 1, wherein said plurality of probes are configured to contact a plurality of semiconductor devices under test, and said electric circuit enhances said test data by receiving test signals from said tester apparatus for testing a first number of semiconductor devices and outputting to said probes test signals for testing a second number of semiconductor devices, wherein said second number is greater than said first number.

Claim 59 (Previously presented): The probe card assembly of claim 1, wherein said daughter card is substantially coplanar to said substrate and there is a space between said daughter card and said substrate.

Claim 60 (Previously presented): The method of claim 19, wherein said plurality of probes are configured to contact a plurality of semiconductor devices under test, and said electric circuit enhances said test data by receiving test signals from said tester apparatus for testing a first number of semiconductor devices and outputting to said probes test signals for testing a second number of semiconductor devices, wherein said second number is greater than said first number.

Claim 61 (Previously presented): The method of claim 19, wherein said daughter card is substantially coplanar to said substrate and there is a space between said daughter card and said substrate.

Claim 62 (Previously presented): The probe assembly of claim 42, wherein said contact means electrically communications with a plurality of semiconductor devices under test, and said electric circuit means enhances said test data by receiving test signals through said printed circuit means for testing a first number of semiconductor devices and outputting to said contact means test signals for testing a second number of semiconductor devices, wherein said second number is greater than said first number.

Claim 63 (Previously presented): The probe assembly of claim 42, wherein said daughter card means is substantially coplanar to said contact means.

Claim 64 (Previously presented): The probe card assembly of claim 50, wherein said plurality of probes are configured to contact a plurality of semiconductor devices under test, and said electric circuit enhances said test data by receiving test signals from said semiconductor tester apparatus for testing a first number of semiconductor devices and outputting to said probes test signals for testing a second number of semiconductor devices, wherein said second number is greater than said first number.

Claim 65 (Previously presented): The probe card assembly of claim 50, wherein said daughter card is substantially coplanar to said substrate and there is a space between said daughter card and said substrate.